What is claimed is:

1. A semiconductor device with two selectable manufacturing configurations, comprising:

a first module layer having a plurality of circuit blocks; and

a second module layer positioned substantially above the first module layer, wherein in a first selectable configuration a plurality of memory circuits are formed to control a portion of the circuit blocks, and wherein in a second selectable configuration a conductive pattern is formed to control substantially the same portion of the circuit blocks.

2. The device of claim 1, further comprising a third module layer positioned substantially above the second module layer, wherein interconnects and routing wires are formed to connect the circuit modules within the first and second module layers.

3. The device of claim 1, further comprising a third module layer positioned between the first and second module layers, wherein interconnects and routing wires are formed to connect the circuit modules within the first and second module layers.

4. The device of claim 1, wherein the second module layer in said first selectable configuration comprises a random access memory (RAM) element.

5. The device of claim 4, wherein the RAM element comprises a user configurable memory.

6. The device of claim 1, wherein the second module layer in said second selectable configuration comprises a read only memory (ROM) element.

7. The device of claim 6, wherein the ROM element comprises a wire connection to a power supply voltage level or a ground supply voltage level.

8. The device of claim 1, wherein the first selectable configuration forms a programmable logic device (PLD), further comprising:

one or more digital circuits formed on the first module layer;

one or more programmable logic blocks formed on the first module layer and electrically coupled to the digital circuits;

one or more memory blocks formed on the first module layer and electrically coupled to the digital circuits;

one or more configurable memory elements formed on the second module layer and electrically coupled to the programmable logic blocks to customize the programmable content of the PLD; and

one or more interconnect and routing wires formed in a third module layer, electrically coupled to first and second module layers to provide the functionality of the PLD.

9. The device of claim 8, wherein the second module layer is generic and user configurable to program and re-program to alter the functional response and performance of the PLD.

10. The device of claim 8, wherein memory is selected from the group consisting of fuse links, laser-fuse links, antifuse capacitors, SRAM cells, DRAM cells, metal optional links, EPROM cells, EEPROM cells, Flash cells, Electro-Chemical elements and Ferro-electric elements.

11. The device of claim 1, wherein the second selectable configuration forms an Application Specific Integrated Circuit (ASIC), further comprising:

one or more digital circuits formed on the first module layer;

one or more programmable logic blocks formed on the first module layer and electrically coupled to the digital circuits;

one or more memory blocks formed on the first module layer and electrically coupled to the digital circuits;

one or more predetermined wire connections formed on the second module layer and electrically coupled to the programmable logic blocks to customize the programmable content; and

one or more interconnect and routing wires formed in a third module layer and electrically coupled to first and second module layers.

12. The device of claim 11, wherein the predetermined wire connections is formed using a bitstream file from the first selectable configuration and wherein the bitstream file is used to map a substantially identical logic control pattern from said first selectable configuration.

13. The device of claim 11, wherein the predetermined wire connections is integrated in the first module layer.

14. The device of claim 11, wherein the predetermined wire connections is integrated in the third module layer.

15. The device of claim 1, wherein for every given memory pattern of the second module layer in the first selectable configuration, a unique predetermined wire connection pattern exists in the second configuration to substantially match logic customization.

16. The device of claim 1, wherein one or more of the circuit blocks within the first module layer maintain substantially identical timing characteristics under both configurations of the second module layer.

17. A programmable logic device, customizable to any one of a plurality of application specific devices, comprised of:

a first module layer comprising a programmable logic circuit; and

a second module layer comprising an interconnect structure wherein interconnects and routing wires are formed to connect the device; and

a third module layer comprising a memory circuit coupled to said programmable logic circuit in the first module layer and the interconnect structure in the second

module layer, said third module layer comprised of two selectable manufacturing configurations, wherein:

a first selectable configuration comprises a random access memory (RAM) element; and

a second selectable configuration comprises a read only memory (ROM) element.

18. The device of claim 17, further comprising:

an input, said input received at an input-pad; and

an output, said output generated at an output-pad; and

an input to output signal propagation delay, said delay substantially identical between said RAM and an equivalent ROM selectable configurations of the third module layer.

19. The device of claim 17, wherein the third module layer in said second selectable configuration is integrated into the second module layer.

20. A semiconductor integrated circuit, comprising:

a digital circuit formed on a substrate; and

a non-planar memory circuit electrically coupled to the digital circuit, said memory circuit being either a random access memory (RAM) constructed to store data to define the logic output of the digital circuit or a read only memory (ROM) conductive pattern constructed to define the logic output of the digital circuit, wherein the RAM and the ROM options provide substantially matching functionality and timing characteristics.